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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,891	10/29/2003	Yoshiyuki Shibata	60188-693	4097

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,891	SHIBATA, YOSHIYUKI	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-21* is/are pending in the application.

4a) Of the above claim(s) *18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claim is 18 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Laurent (U.S. Patent No. 6,418,044).

In re claim 13, Laurent discloses a semiconductor device (see entire disclosure, especially, abstract, column 1, lines 38-50), comprising a first DRAM section including a first memory cell having a first capacitance and a second DRAM section including a second memory cell having a second capacitance different from the first capacitance (abstract), the first DRAM section and the second DRAM section being provided on the same semiconductor substrate,

wherein the first memory cell has a first capacitive element including a first capacitor lower electrode, a first capacitor insulting film, and a first capacitor upper electrode (the examiner notes that a capacitor must have these elements),

the second memory cell has a second capacitive element including a second capacitor lower electrode, a second capacitor insulating film, and a second capacitor upper electrode (the examiner notes that a capacitor must have these elements), and

an operating voltage of the first DRAM section is different from an operating voltage of the second DRAM section (see column 1, lines 35-50 and Figure 1, reference cell operating at voltages lower than ½ V_{DD} and ground, whereas the memory cell operates at voltages between V_{DD} and ground).

In re claim 19, Laurent discloses the method wherein the first DRAM section and the second DRAM section are formed on the same chip (see column 3, lines 5-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-15, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent No. 5,814,547) in view of applicant's admitted prior art ("AAPA" see specification pages 1-5 and Figures 12A-12C).

In re claim 13, Chang discloses a semiconductor device, comprising a first DRAM section including a first memory cell having a first capacitance and a second DRAM section including a second memory cell having a second capacitance different

from the first capacitance, the first DRAM section and the second DRAM section being provided on the same semiconductor and wherein the first memory cell has a first capacitive element including a first capacitor lower electrode, a first capacitor insulting film, and a first capacitor upper electrode (substrate, 50, 52 of center capacitor) and the second memory cell has a second capacitive element including a second capacitor lower electrode, a second capacitor insulating film, and a second capacitor upper electrode substrate (substrate, 50, 52 of right hand side capacitor; see column 3, lines 15-30 and Figure 11).

Chang discloses the device as claimed and rejected above, but does not disclose the method wherein the first DRAM section with lower capacitance has a higher operating voltage than that of the second DRAM section with higher capacitance. AAPA discloses that devices for use with portable terminals have a plurality of DRAM sections formed on the same semiconductor substrate have different operating voltages (see specification page 4) and conventional DRAM embedded LSI chips have a first DRAM section that needs to operate at high speed and a second DRAM section that is intended to operate at low power consumption with a sufficient signal holding characteristic (see specification, page 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first DRAM section with lower capacitance of Chang to operate at a higher operating voltage than that of higher capacitance second DRAM section in order to allow for a higher operating speed for first DRAM section because less charge is required to be moved, while allowing for a sufficient signal holding characteristic for the second DRAM section because of since a

large amount of charge may be stored. The examiner notes the definition of the capacitance as defined in Merriam Webster's Collegiate Dictionary, Tenth edition, as the measure of the property that is equal to the ratio of the charge on either surface to the potential difference between the surfaces.

In re claim 19, Chang discloses the method wherein the first DRAM section and the second DRAM section are formed on the same chip (see Figure 11).

In re claim 20, the combined Chang and AAPA disclose the method wherein the charge stored in the first capacitive element is smaller than charge stored in the second capacitive element (see specification, page 2).

Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laurent (U.S. Patent No. 6,418,044) in view of Figura (U.S. Patent No. 5,696,014).

Laurent discloses the method as claimed and rejected above including forming two different capacitors on a single substrate with different capacitances (abstract), but does not disclose the method wherein the first capacitor lower electrode is composed of a diffusion layer formed in the semiconductor substrate and the second capacitor lower electrode is composed of a conductive film formed on the insulating film provided on the substrate or the method wherein the first capacitive element has a structure of a planar capacitor and the second capacitive element has a structure of a stacked capacitor.

Figura discloses the method of forming capacitors, wherein a first capacitor lower electrode is composed of a diffusion layer (17, see Figure 1 or 2) formed in the semiconductor substrate and another second capacitor lower electrode is composed of

a conductive film (32) formed on the insulating film provided on the substrate (see Figure 3) or the method wherein a first capacitive element has a structure of a planar capacitor (see Figure 1) a second capacitive element has a structure of a stacked capacitor (see Figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitors by the method of Figura, because as Laurent teaches the capacitance of the devices are desired to be different, and Figura teaches conventional methods of forming capacitors with different capacitances, (i.e. planar or stacked capacitors).

Claim 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laurent (U.S. Patent No. 6,418,044) in view of Pan (U.S. Patent No. 5,858,832).

Laurent discloses the method as claimed and rejected above but does not disclose the method of forming the memory cell wherein the first memory cell includes a gate insulting film formed on the semiconductor substrate and a gate electrode formed on the gate insulting film and the first capacitor insulating film is made of the same insulating film as the gate insulating film.

Pan discloses the method of forming the memory cell wherein the first memory cell includes a gate insulting film formed on the semiconductor substrate and a gate electrode formed on the gate insulting film and the first capacitor insulating film is made of the same insulating film as the gate insulating film (see column 5, lines 20-55). It would have been obvious to one of ordinary skill in the art at the time the invention was

made to form the gate insulting layer and the insulating layer of the planar capacitor of the same insulating film because it allows for reduction in process steps.

Response to Arguments

Applicant's arguments, see page 4, lines 10 through page 5, lines 15), filed October 26, 2004, with respect to the 102/103 rejection of Oowaki have been fully considered and are persuasive.

The Applicant's arguments filed October 26, 2004 with respect to the 102/103 rejection with Chang have been fully considered but they are not persuasive. Applicant argues that since Chang expressly discloses the lower electrode is common in the substrate that different operating voltages cannot be applied. The examiner notes that Chang teaches that the capacitors are formed separate from each other with "each" having a different capacitance. They must be separate from each other to each have a different capacitance and to operate separately. The examiner notes that the Figure 11 shows an uncompleted device, just as Figure 6 shows an uncompleted device. Further steps such as isolation must be made in order to create an operable device.

Conclusion

The examiner notes that Applicant elected Embodiment I and Group I in the Response to Restriction Requirement filed 5/12/2004. The support for the newly added claims relied upon non-elected embodiments. The examiner requests Applicant's

cooperation in that support be documented for the elected embodiment in the elected embodiment's corresponding figures and the specification.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk